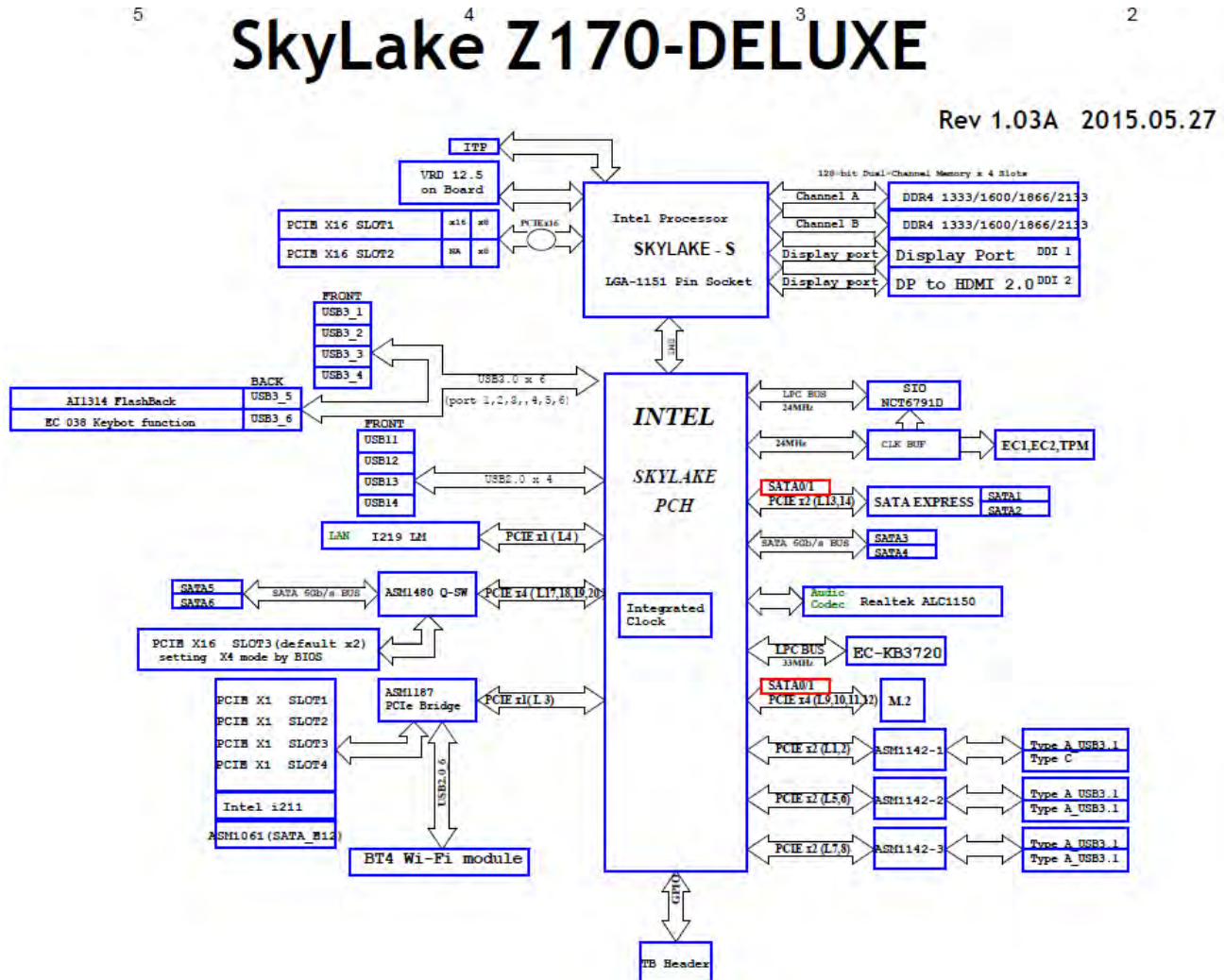
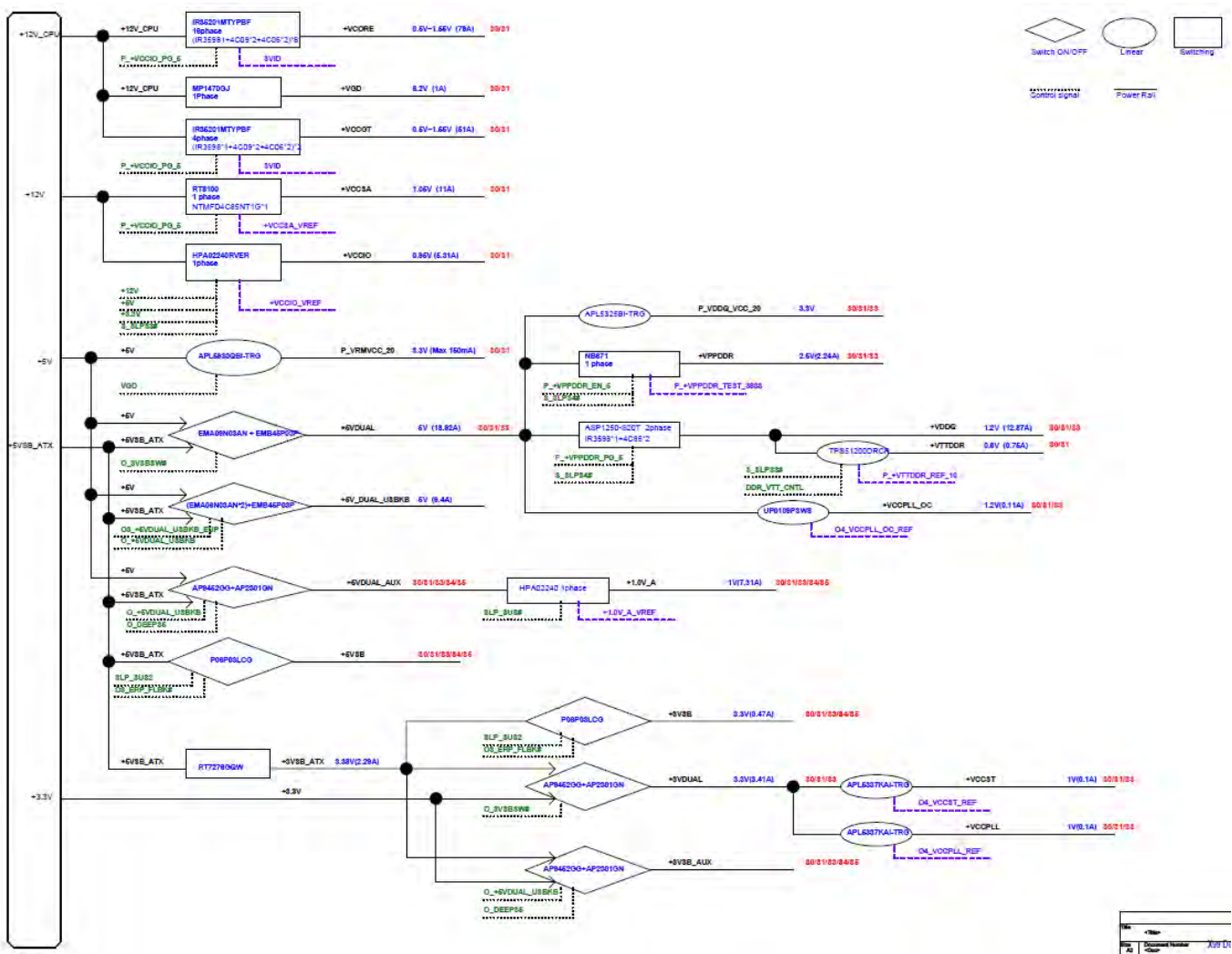


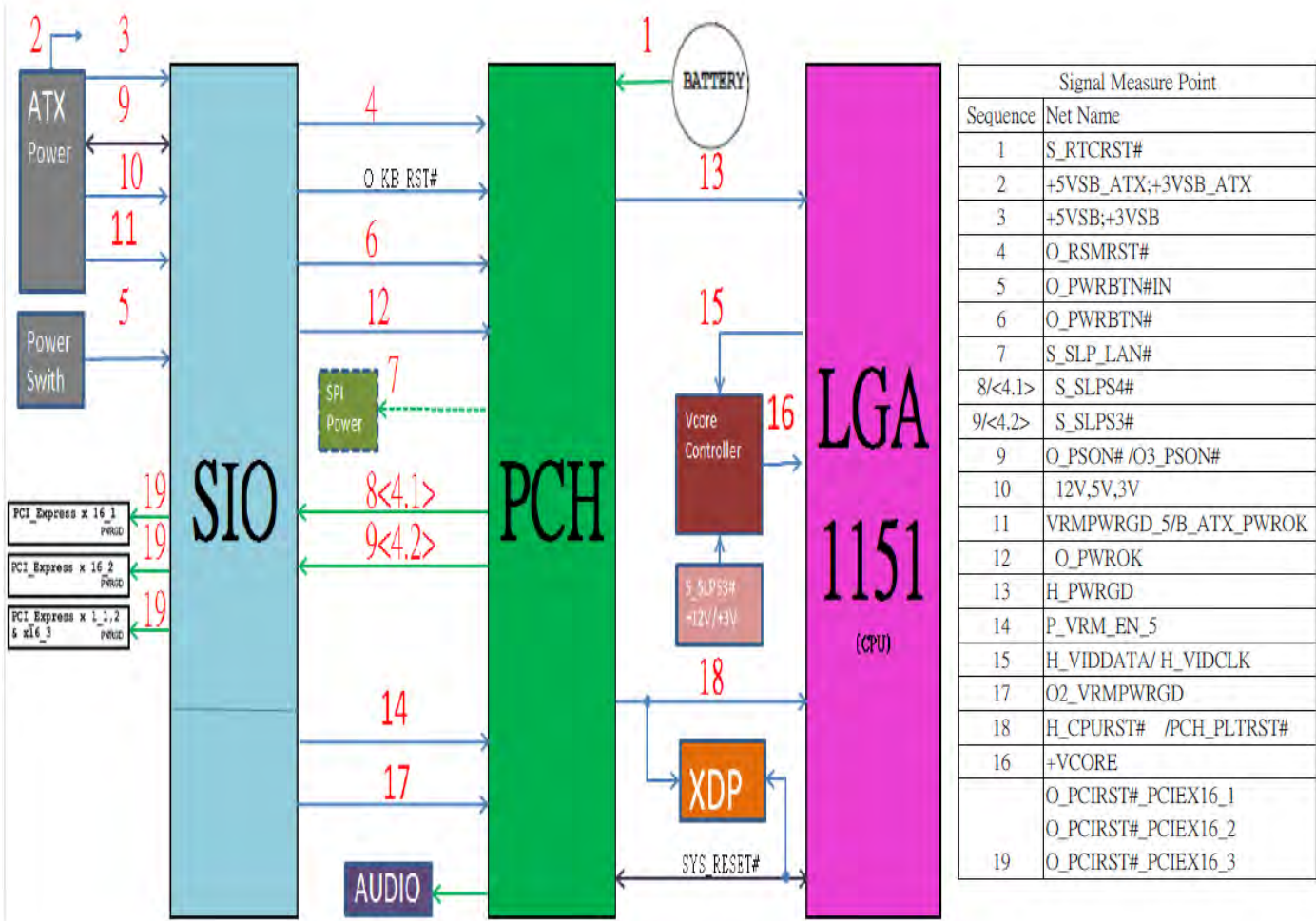
## 1. BLOCK DIAGRAM



## 2. POWER FLOW

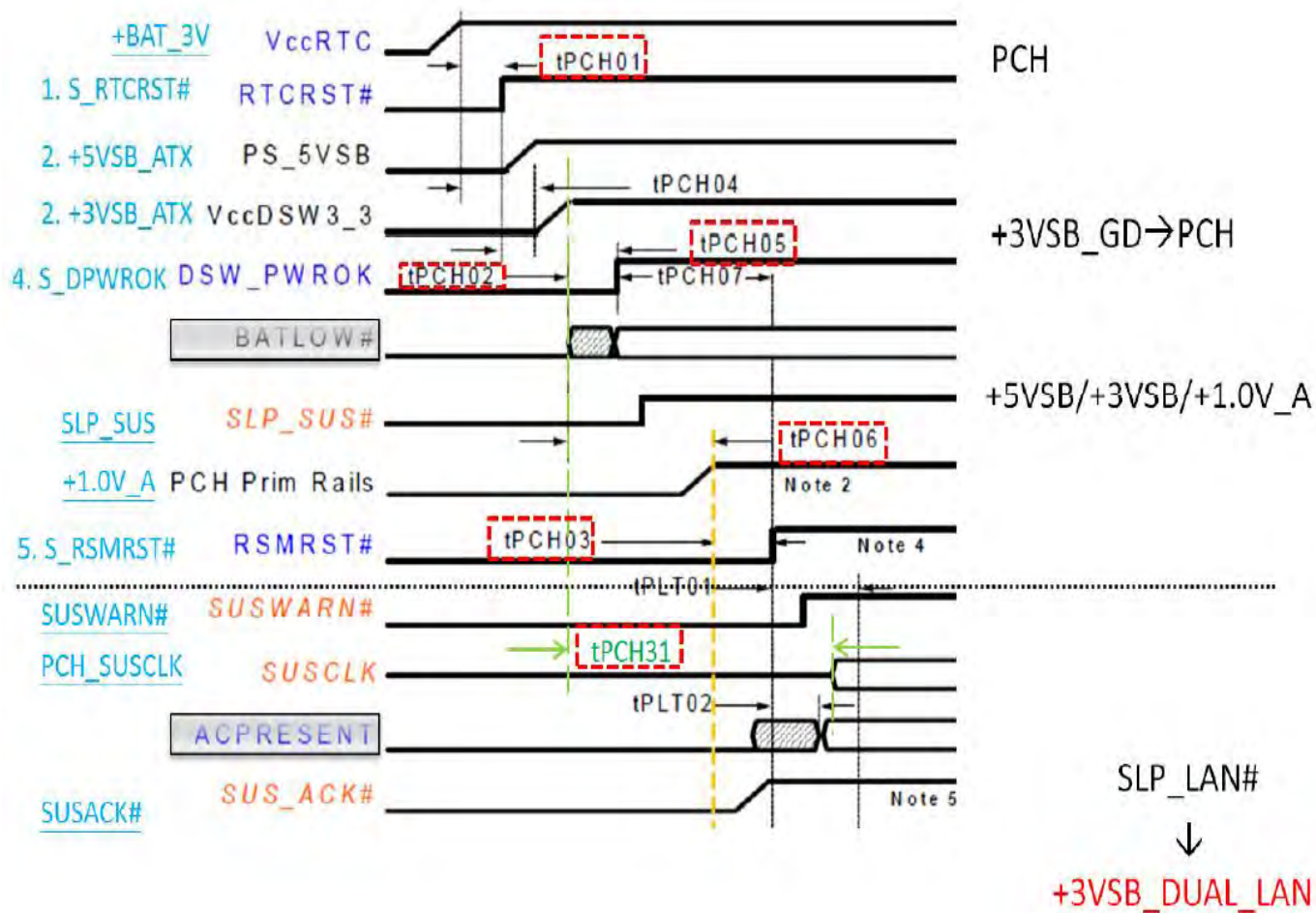


3. POWER ON SEQUENCE



#### 4. Timing Diagram for G3 to S5

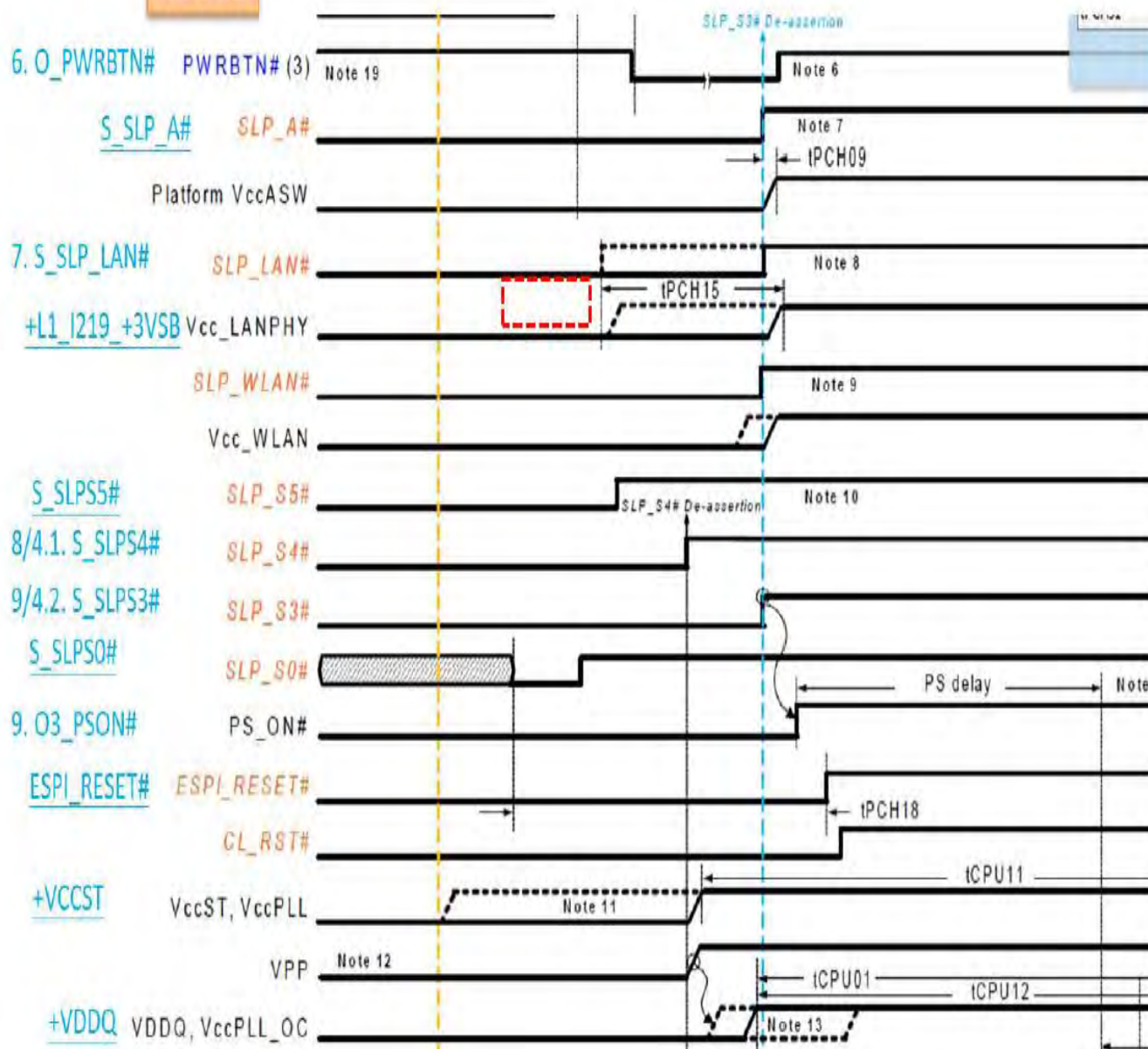
G3→S5

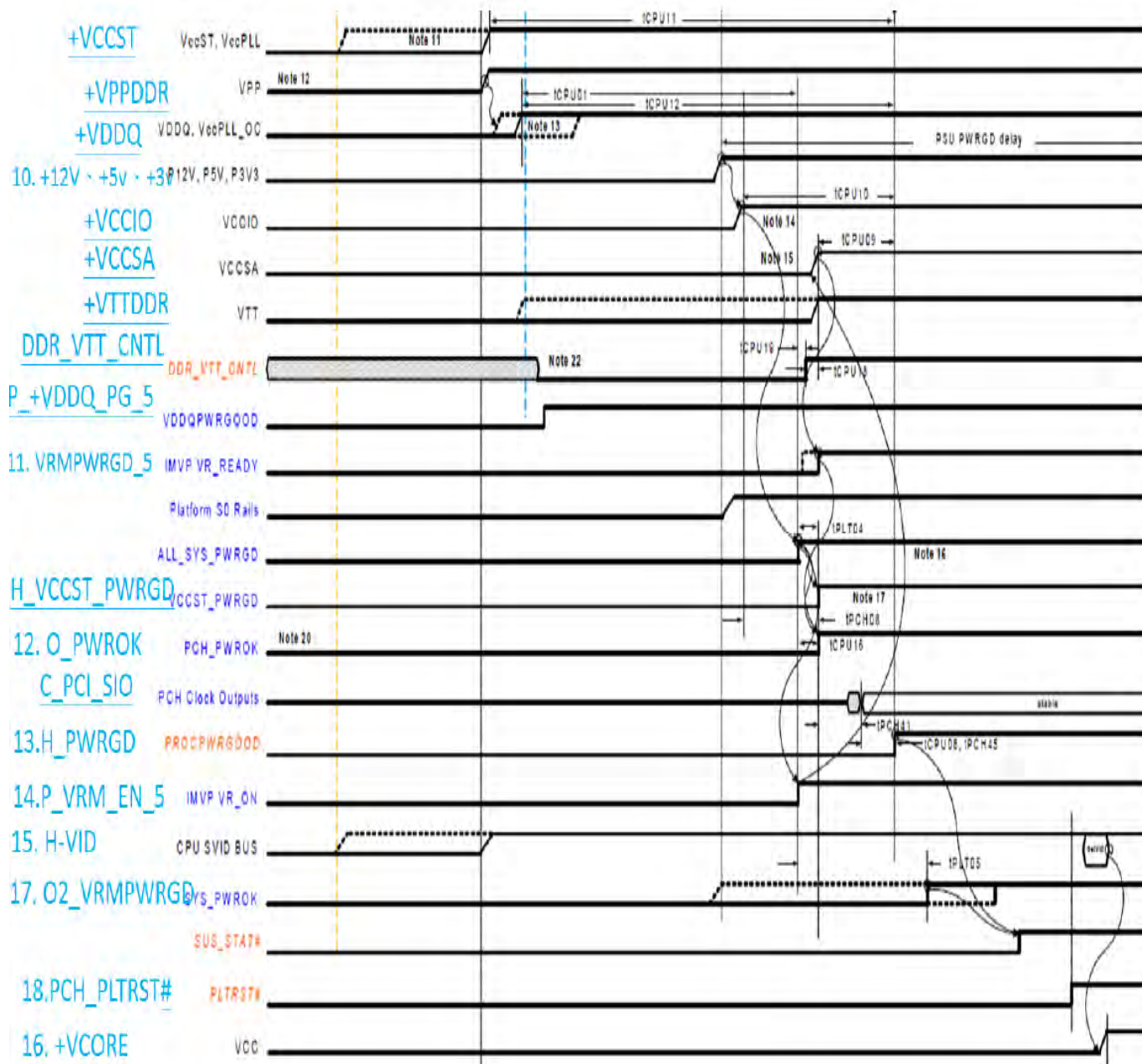




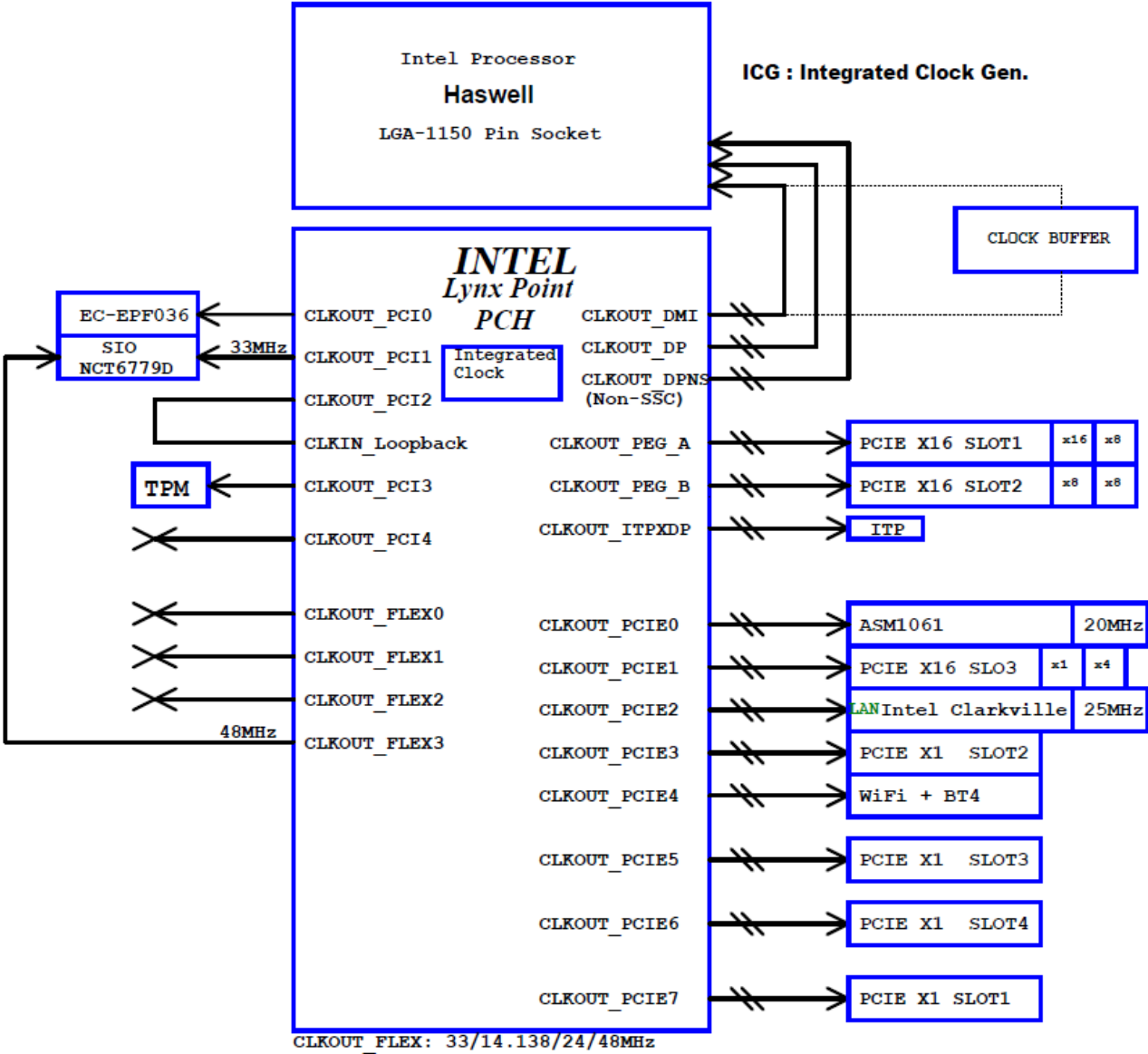
## Timing Diagram for S5 to S0/M0

S5→S0





5. Frequency Flow



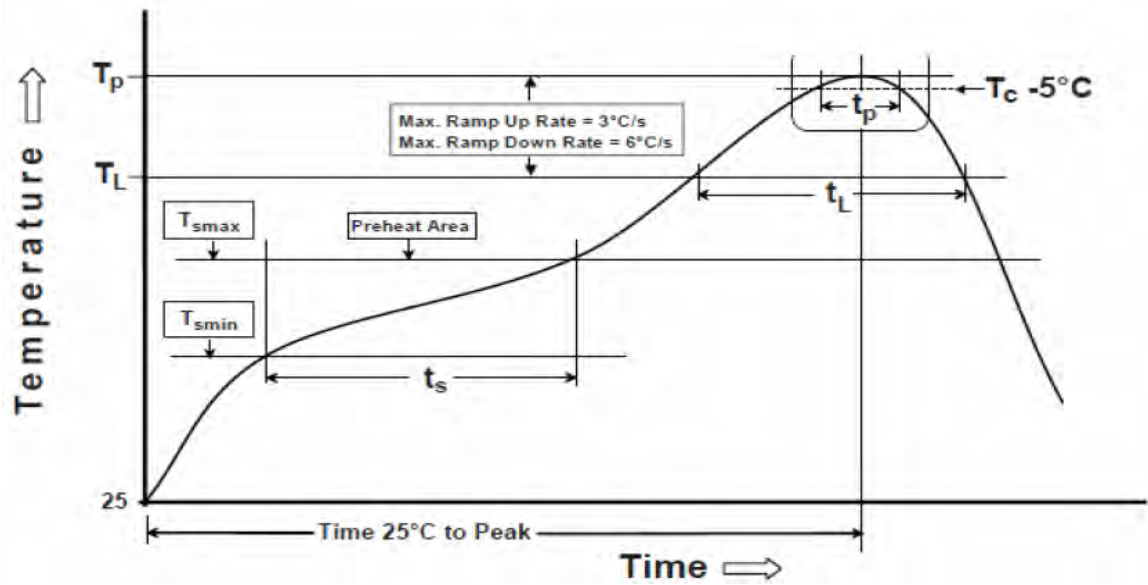
6. Socket reflow profile

Profile Feature	SMD Pb-Free Assembly	DIP Pb-Free Assembly	SMT Component Vendor Spec	DIP Component Vendor Spec
Preheat/Soak				
Temperature Min (T <sub>min</sub> )	150 °C	80 °C	150 °C	135 °C
Temperature Max (T <sub>max</sub> )	200 °C	135 °C	200 °C	need endure 80 seconds
Time (t <sub>s</sub> ) from (T <sub>min</sub> to T <sub>max</sub> )	120 seconds	120 seconds	need endure 120 seconds	
Ramp-up rate (TL to Tp)	3 °C/second max.	3 °C/second max.	need endure 3 °C/second max.	need endure 3 °C/second max.
Liquidous temperature (TL)	217 °C	NA	217 °C	NA
Time (t <sub>L</sub> ) maintained above TL	90 seconds		need endure 90 seconds	
Peak package body temperature (Tp)	260 °C	270 °C	260 °C	270 °C
Time (tp)* within 5 °C of the specified classification temperature (Tc), see Figure 1-1 .	10* seconds	6* seconds	need endure 10* seconds	need endure 6* seconds
Ramp-down rate (Tp to TL)	6 °C/second max.	6 °C/second max.	need endure 6 °C/second max.	need endure 6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.	8 minutes max.	8 minutes max.	8 minutes max.

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ± 2 °C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

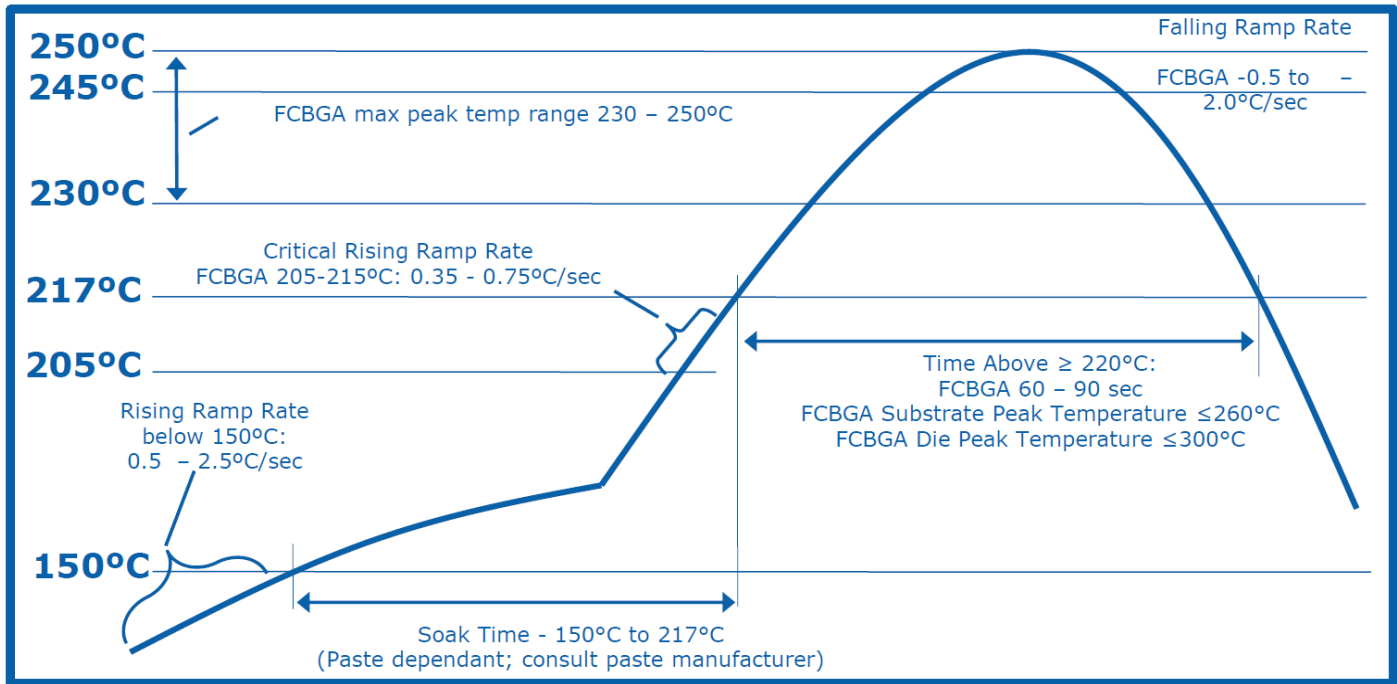
2. DIP Plastic heat resistance capability :

- (1) Direct contact 270°C, 6 seconds
- (2) In-direct contact 230°C, 5 seconds
- (3) no contact 130°C, 5 seconds





## 7. Lead-Free Rework Thermo profile Graphic for BGA & Chipset



Except for body temp, all temperatures are measured with thermo couples inside solder joints, for better accuracy

### Primary Factors for Successful Rework:

- Flux formulation and solder paste formulation and volume
- A capable thermal reflow profile
- Proper PCB pad solder preparation/wicking (clean-up of the residual solder from the PCB pads)

**Caution: Always remove batteries and thermal solutions following the system design disassembly process steps prior to BGA rework to avoid damaging the BGA.**

View this Intel®BGA / Socket Rework Video (10 minutes in length):

<http://link.brightcove.com/services/player/bcpid1409165005001?bckey=AQ~~,AAAQwZd9wk~,X1Exj3sUi-03b71FGkEmVWbi4T4yGcor&bctid=1519232885001>

8. MB Baking Time: 120 °C, 8 hours

BGA Baking Time:

**5.2 Floor Life** The floor life of SMDs per Table 5-1 will be modified by environmental conditions other than 30 °C/60% RH. Refer to Clause 7 to determine maximum allowable time before rebake would be necessary. If partial lots are used, the remaining SMD packages must be resealed or placed in safe storage within one hour of bag opening (see 5.3). If one hour exposure is exceeded, refer to 4.1.

Table 5-1 Moisture Classification Level and Floor Life per J-STD-020

Level	Floor Life (out of bag) at factory ambient ± 30 °C/60 % RH or as stated
1	Unlimited at ± 30 °C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Supplier Bake: Default Baking Times Used Prior to Dry-Pack that were Exposed to Conditions ± 60 % RH (“MET” = 24 h )

Package Body Thickness	Level	Bake @ 125° C +10/-0 ° C	Bake @ 150° C +10/-0 ° C
≤ 1.4 mm	2	7 hours	3 hours
	2a	8 hours	4 hours
	3	16 hours	8 hours
	4	21 hours	10 hours
	5	24 hours	12 hours
	5a	28 hours	14 hours
> 1.4 mm ≤ 2.0 mm	2	18 hours	9 hours
	2a	23 hours	11 hours
	3	43 hours	21 hours
	4	48 hours	24 hours
	5	48 hours	24 hours
	5a	48 hours	24 hours
> 2.0 mm ≤ 4.5 mm	2	48 hours	24 hours
	2a	48 hours	24 hours
	3	48 hours	24 hours
	4	48 hours	24 hours
	5	48 hours	24 hours
	5a	48 hours	24 hours

**Note 1:** If baking of packages > 4.5 mm thick is required see appendix B.

**Note 2:** The bake times specified are conservative for packages without blocking planes or stacked die. For a stacked die or BGA package with internal planes that impede moisture diffusion the actual bake time may be longer than that required in Table 4-2 if packages have had extended exposure to factory ambient before bake. Also the actual bake time may be reduced if technically justified. The increase or decrease in bake time **shall** be determined using the procedure in JEDEC JESD22-A120 (i.e., < 0.002 % weight loss between successive readouts) or per critical interface concentration calculations.

**9. Voltage Measure Point**

Voltage Measure Point		
Station	Net Name	Diode resistance
OR1009	+3VSB_ATX	315
MU3009	+VCCCMP	255
D3R10	+5VSB	467
PC1088	+VGD	432
PC741	+VCCGT	441
EATX12V	12V_CPU	600
PL401	+VCCSA	452
TPM	+3VSB	284
PQ607	+5V_DUAL_USBKB	376
PU202	+VTTDDR	414
EATXPWR	+5VSB_ATX	479
PQ602	+5VDUAL	352
EATXPWR	+12V	521
EATXPWR	+5V	420
EATXPWR	+3V	193

## 10.Signal Measure Point

		Signal Measure Point	
Station	Sequence	Net Name	Diode resistance
SR119	1	S_RTCRST#	778
SR120		S_SRTCST#	778
NA	2	AC Power Switch ON	NA
D3R10	3	+5VSB	467
TPM		+3VSB	284
SR142	3.1	S_DPWROK	18
SR142	4	O_RSMRST#	18
PANEL	5	O_PWRBTN#IN	500
SC29	6	O_PWRBTN#	443
SD5	7/4.2	S_SLP_S3#	495
NA	7	S_SLP_A#	NA
NA	7.1	S_SLP_LAN#	NA
PQ3011	8/4.1	S_SLP_S4#	500
OR211	9	O_PSON#	549
EATXPWR	10	12V	521
EATXPWR		5V	420
EATXPWR		3V	193
EATXPWR	11	B_ATX_PWROK	568
SQ40	12	O_PWROK	541
SR75	13	H_PWRGD	440
HR210	14	H_VIDDATA	361
PR109		H_VIDCLK	362
PC1103	15	+VCORE	398
PQ3002	16	VRMPWRGD_5	497
TPM	17	S_PLTRST#	422
HQ8	18	H_CPURST#	389
XC71	19	O_PCIRST#_PCIEX16_1	546
XC72		O_PCIRST#_PCIEX16_2	546